In the Drawings

The Examiner objected to Applicants' Drawings for failing to show every feature of the invention specified in the claims. The Examiner is requested to enter new Figures 7 and 8 added in response to the objection and provided herewith. New Figure 7 includes an etched substrate, and new Figure 8 includes a semiconductor device formed on the substrate. New Figures 7 and 8 are supported by the specification at page 6, lines 25-30. No new matter was added.

In the Specification

Please amend the paragraph beginning at page 5, line 16 to recite as follows:

Next, metallic germanium layer 22 is patterned by etching through the photolithography image formed by photo resist layer 24. A reactive ion etching (RIE) process is preferably used to etch metallic germanium layer 22. Other etching process having a high etch selectivity between metallic germanium and photo resist can also be used to etch metallic germanium layer 22 through the mask formed by photo resist layer 24. Because of high the etch selectivity of metallic germanium relative to photo resist, photo resist layer 24 can be a thin layer of photo resist material. The thickness of photo resist layer 24 can further reduced by using a thin layer 22 of metallic germanium, thereby shortening the metallic germanium etching process. A thin photo resist mask is compatible with a shallow depth of focus photolithography processes, and therefore is preferred in the fabrication of semiconductor devices with small features. After etching layer 22 of metallic germanium, photo resist layer 24 is stripped away using techniques known in the art. The remaining germanium serves as a metallic germanium hard mask 25 over of dielectric stack 15 as shown in FIG. 3. Germanium hard mask 25 has openings, e.g., openings 26 shown in FIG. 3, through which dielectric stack 15 is selectively etched in a subsequent step of the etching process.